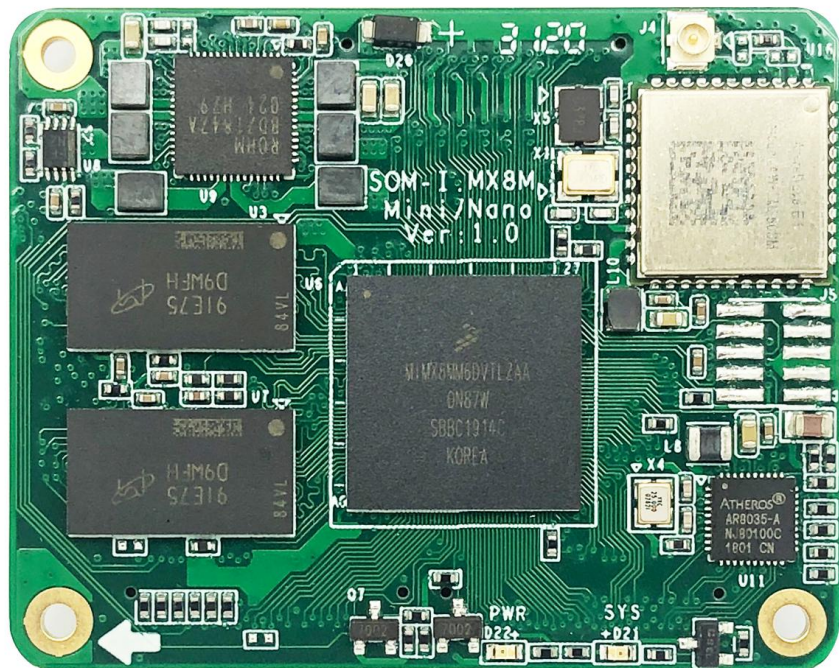
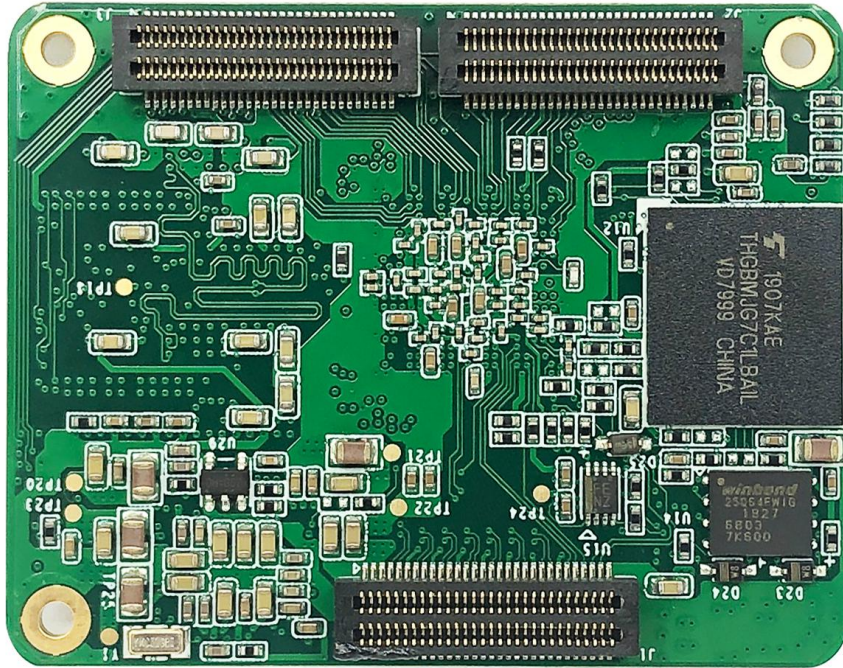


SOM-IMX8M-MINI





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1. General

This document describes the hardware architecture of the SOM-IMX8M-MINI Module.

The IMX8M-MINI System-On-Module (SOM) board is based on NXP's energy efficient i.MX 8M Mini processor which has up to 4 x Cortex-A53 cores capable at running up to 1.8 GHz and one Cortex-M4 core capable at running up to 400 MHz core for low-power and real-time operation.

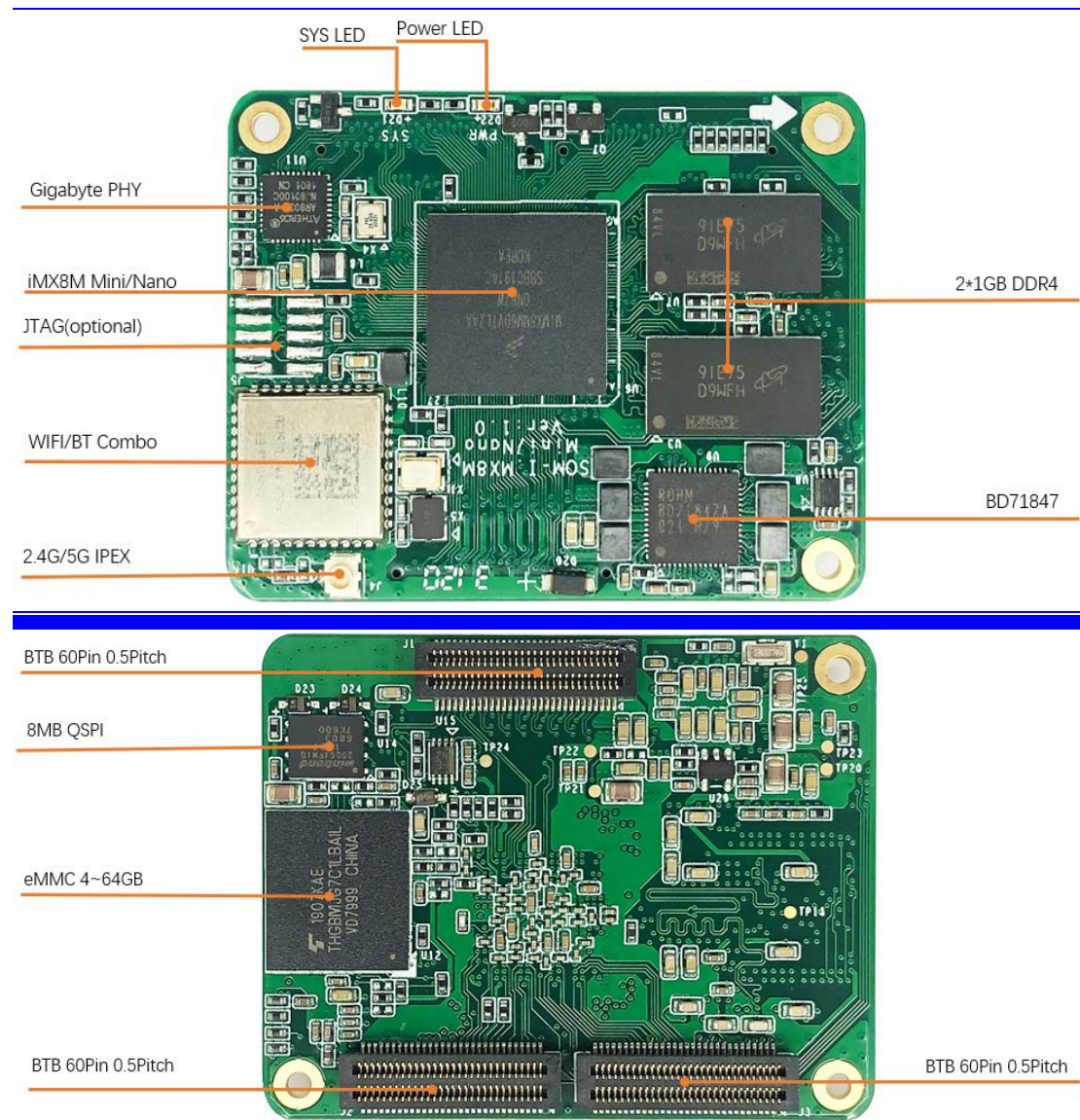
On-board up to 4GB DDR, up to 64GB eMMC and a WiFi / Bluetooth module, and with MIPI DSI display output, MIPI CSI camera inputs, flexible audio interfaces and comprehensive communication features. The SOM-IMX8M-MINI Module is a fully-integrated system that helps you build your professional embedded systems rapidly.

Support Linux kernel, Yocto Project file-system, Debian and Android run on the Cortex-A core, and Real-time OS such as UCOS and FreeRTOS run on the Cortex-M core.

Comes with detailed user manual, ready-made system, and friendly technology support. We are able to provide customize based on this SOM module for various application.

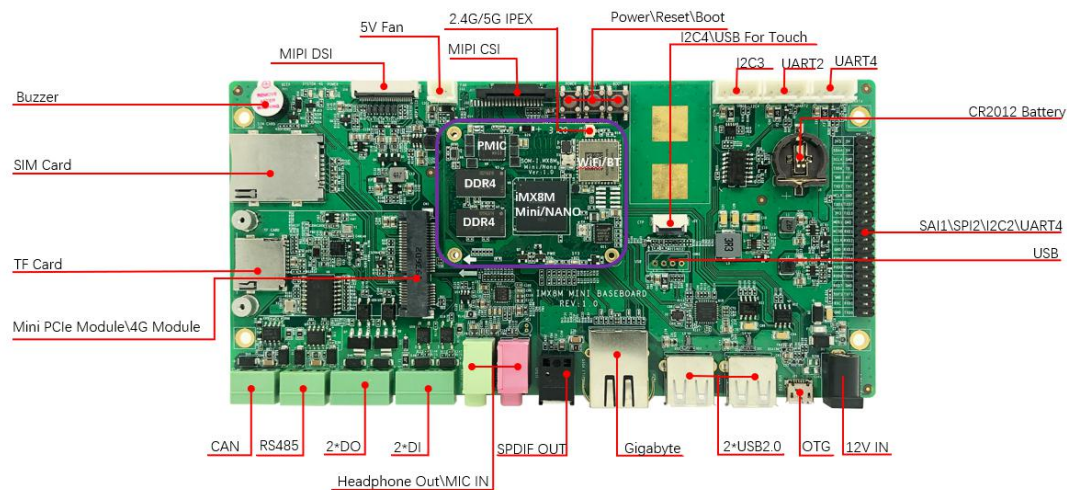
2. Features

2.1 SOM-IMX8M (MINI AND NANO)



- NXP i.MX8M MINI SOC
 - Quad-core ARM Cortex-A53, plus Cortex-M4
 - 64-bit Armv8-A architecture
 - 2D/3D GC520L
 - Media Processing Engine (MPE) with NEON technology
 - Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
 - Target frequency up to 1.8GHz
- Wi-Fi 1x1 (802.11b/g/n/ac 2.4/5GHz)
- Bluetooth 5.0
- From 8 to 64GB eMMC
- From 1 to 4GB DDR4
- 64M bit Quad SPI Flash on-board

2.1 SBC-IMX8M



- USB 2.0 Host x 2
- USB OTG x 1
- 12V Power IN x 1
- Up to 77xGPIO (including SPI,I2C,PWM,UART,SAI, and SDIO)
- USB 2.0 Host (4 Pin Connector) x 1
- UART:

- UART2 (TTL, For Debug)
 - UART3 (TTL, For User)
 - UART4 (TTL, For User)
- I2C x 3
- USB Touch x 1
- MIPI-CSI-2 x 1
- Fan 5V port x 1
- MIPI-DSI x 1
- Buzzer x 1
- SIM Card x 1
- TF Card x 1
- Mini PCIE Interface x 1, For 4G module and PCIE module
- CAN Bus x 1
- RS485 Bus x 1
- Input Terminal x 2 PIN (With Isolation)
- Output Terminal x 2 PIN (With Isolation)
- Headphone Output/MIC In x 1
- SPDIF Out x 1
- 1x Gigabit Ethernet on-board

3. Hardware Overview

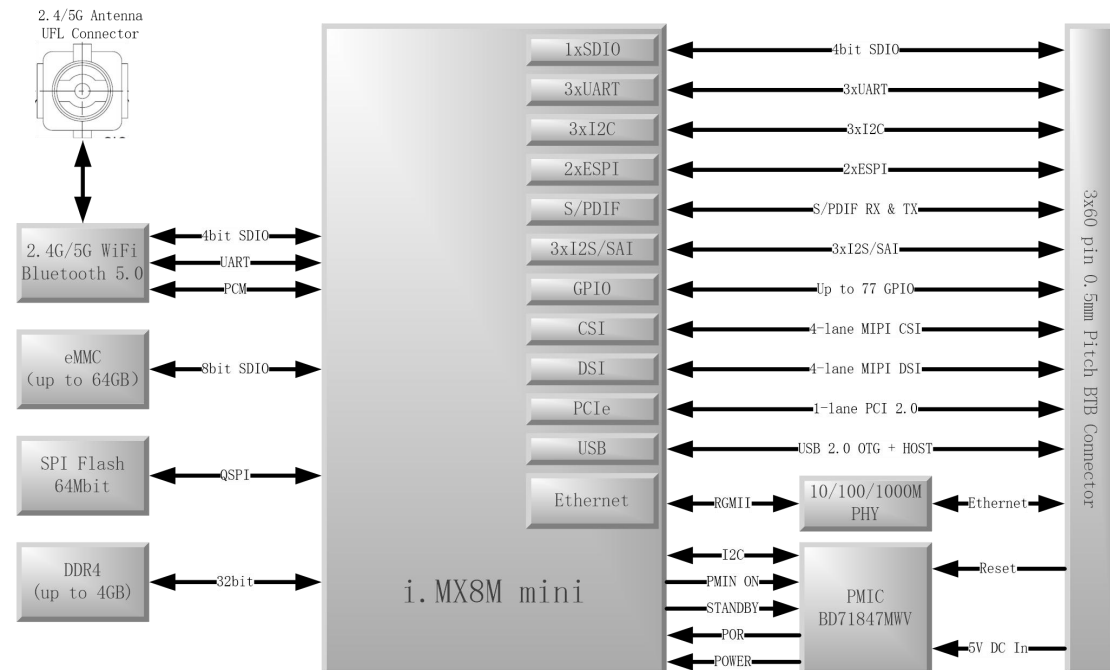
3.1 System Components

Feature	Details
i.MX8M MINI SOC	
Arm Cortex-A53 MPCore platform	Quad symmetric Cortex-A53 processors, including: • 32 KB L1 Instruction Cache • 32 KB L1 Data Cache • Media Processing Engine (MPE) • Floating Point Unit (FPU) Support of 64-bit Armv8-A architecture • 512 KB unified L2 cache • Target frequency of 1.8GHz
Arm Cortex-M4 core platform	• 16 KB L1 Instruction Cache • 16 KB L1 Data Cache • 256 KB TCM
Graphic Processing Unit (GPU)	• GC NanoUltra frequency up to 800 MHz • OpenGL ES 2.0 • 2D GC520L
Video Processing Unit (VPU)	• VP9,VP8,AVC,H.265,H.264 decoder • VP8, AVC,H.264 encoder
Audio	• S/PDIF Input and Output • SAI modules supporting I2S,AC97,TDM
On-chip memory	• Boot ROM (256KB) • On-chip RAM (256KB + 32KB)
Memory and storage	
DDR SDRAM	• 2GB DDR4 SDRAM (32-bit bus width) • 1200MHz maximum DDR clock • Interfaces directly to the iMX8M MIPI build-in DDR controller
eMMC	• 8GB NAND eMMC flash memory • 8-bits MMC mode • Conforms to JEDEC version 5.0 and 5.1

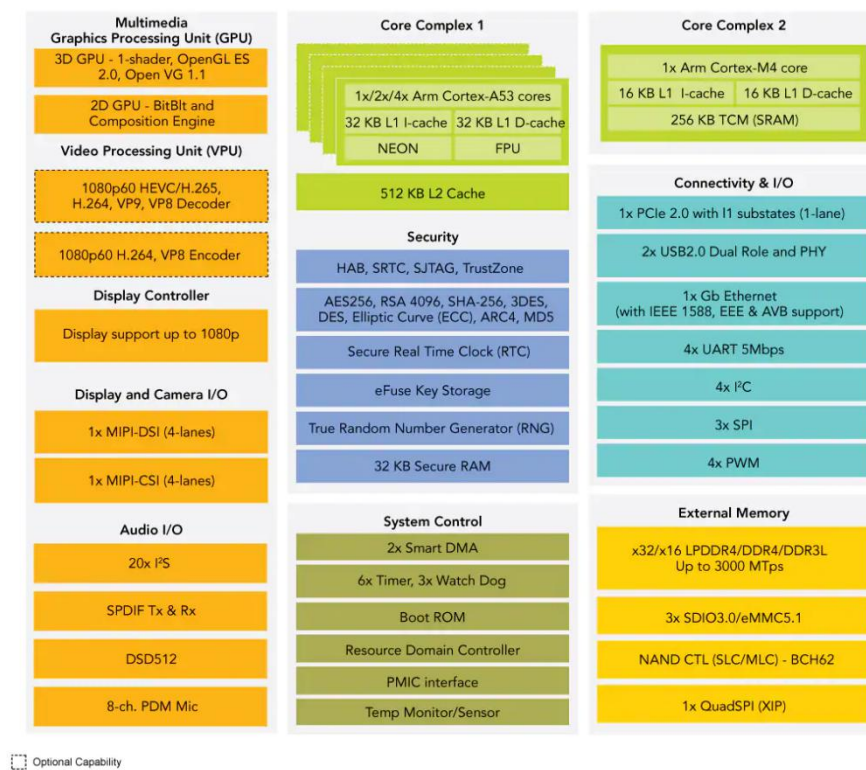
SPI Flash	• 64M bit SPI flash memory • 104MHz Single, Dual/Quad SPI clocks • More than 100,000 erase/program cycles • More than 20-year data retention
Expandable flash (MicroSD)	• Meets SD/SDIO 3.0 standard Runs at 4-bits • Supports system boot from SD card
Network & Wireless	
Ethernet	• On-board 10/100/1000 Mbps Ethernet PHY
Wi-Fi	AzureWave AW-CM256SM module: • Wi-Fi 1x1 (802.11a/b/g/n/ac 2.4/5GHz) • SDIO 3.0 • High speed wireless connection up to 433.3Mbps
Bluetooth	AzureWave AW-CM256SM module: • Bluetooth 5.0 (supports Bluetooth low-energy) • High-speed UART • PCM audio
Hardware Interface	
I/O connectivity	• 1x single lane PCI Express Gen 2 • 2x USB2.0 OTG with integrated PHY • 1x SDIO supporting MMC 5.1, SDIO 3.01 • 1x Gigabit Ethernet with integrated PHY • 3x UART • 3x I2C • 2x ESPI
Display Interfaces	• 4-lane MIPI DSI interface
Camera	• 4-lane MIPI CSI interface

3.2 Functional Block Diagrams

The following figure is a functional block diagram of the IMX 8M MINI SOM:



Functional Block Diagrams

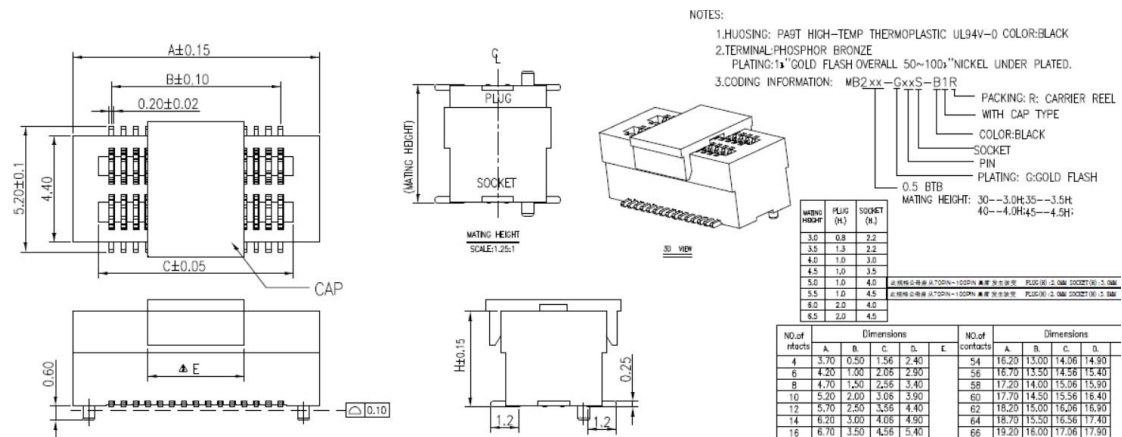


i.MX 8M Mini system block diagram

3.3 Interface Description

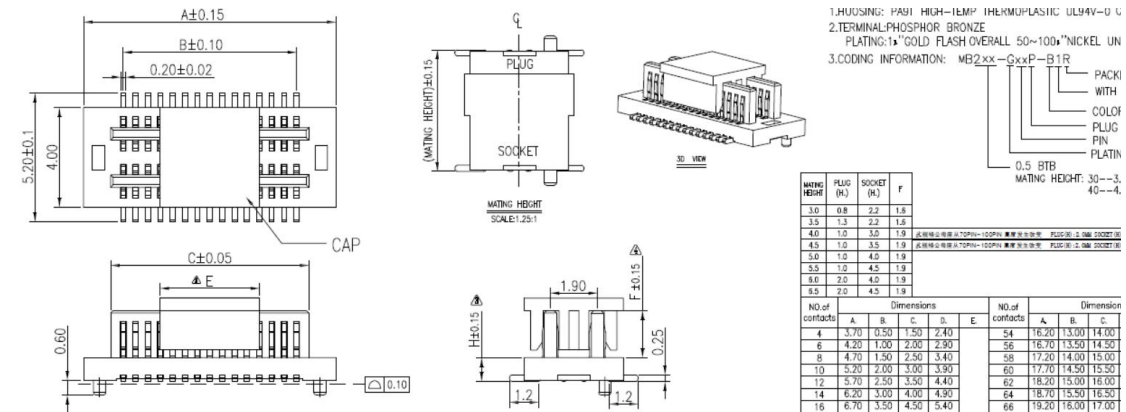
3.3.1 BTB Expansion Connector

The BTB connector mounted on SOM is MB250-G60S-B1R supplied by MTCNN. The detail of the connector is:



Connector Specifications For SOM

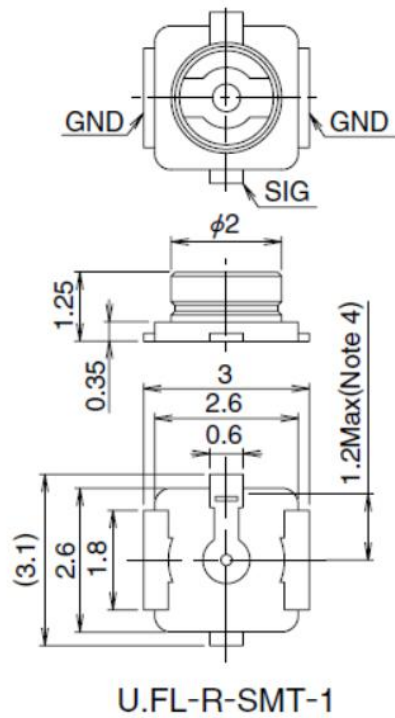
The recommended BTB connector can be mounted on baseboard is MB250-G60P-B1R supplied by MTCNN , The detail of the connector is as following:



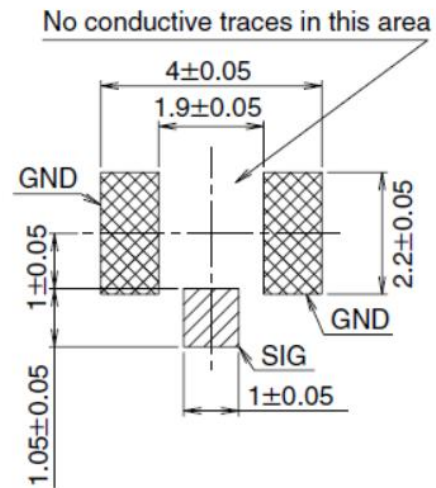
Connector Specifications For Baseboard

3.3.2 WiFi/BT Antenna Connector

The antenna connector mounted on SOM is Ultra Small Surface Mount Coaxial Connector, the detail of the connector is as following:

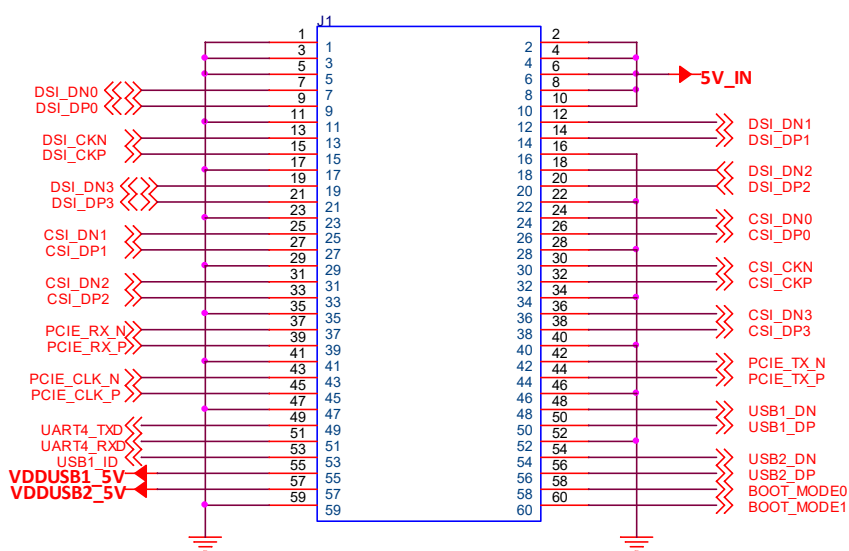
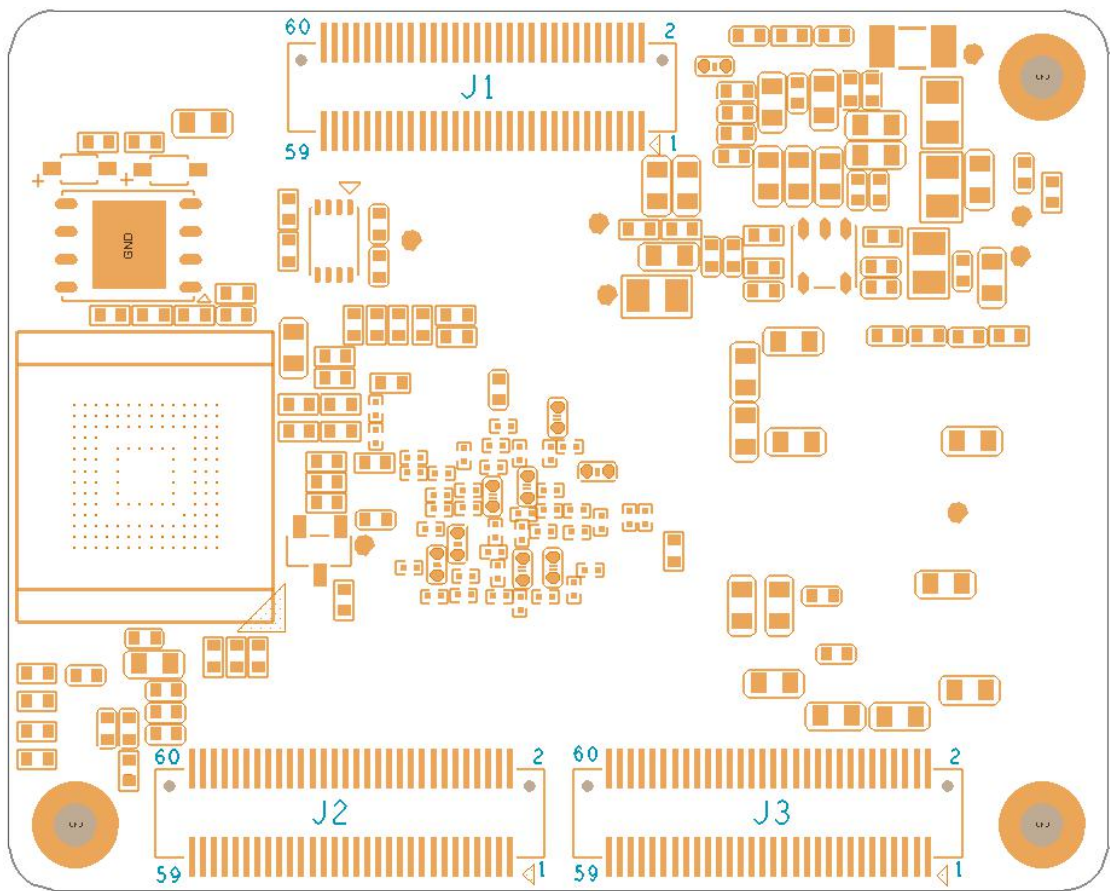


Recommended PCB Mounting Pattern



Specifications For UFL

3.3.3 Pinout Description Table

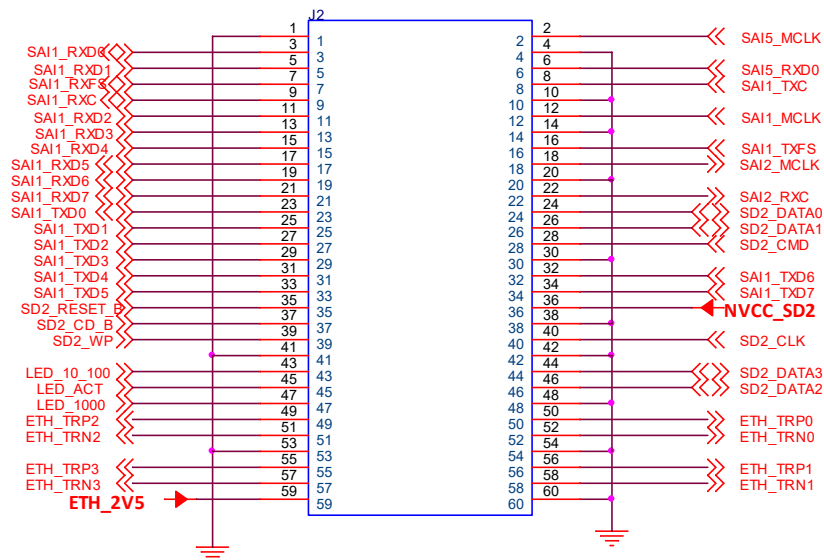


J1

Table1 Pin Definition Of J1

J1					
Number	Signal	Power Logic	Input/Output	CPU Ball	Note
1	GND				
2	5V_IN		Power In		
3	GND				
4	5V_IN		Power In		
5	GND				
6	5V_IN		Power In		
7	DSI_DN0	MIPI DSI		A9	
8	5V_IN		Power In		
9	DSI_DP0	MIPI DSI		B9	
10	5V_IN		Power In		
11	GND				
12	DSI_DN1	MIPI DSI	Output	A10	
13	DSI_CKN	MIPI DSI	Output	A11	
14	DSI_DP1	MIPI DSI	Output	B10	
15	DSI_CKP	MIPI DSI	Output	B11	
16	GND				
17	GND				
18	DSI_DN2	MIPI DSI	Output	A12	
19	DSI_DN3	MIPI DSI	Output	A13	
20	DSI_DP2	MIPI DSI	Output	B12	
21	DSI_DP3	MIPI DSI	Output	B13	
22	GND				
23	GND				
24	CSI_DN0	MIPI CSI	Input	A14	
25	CSI_DN1	MIPI CSI	Input	A15	
26	CSI_DP0	MIPI CSI	Input	B14	
27	CSI_DP1	MIPI CSI	Input	B15	
28	GND				
29	GND				
30	CSI_CKN	MIPI CSI	Input	A16	
31	CSI_DN2	MIPI CSI	Input	A17	
32	CSI_CKP	MIPI CSI	Input	B16	
33	CSI_DP2	MIPI CSI	Input	B17	
34	GND				
35	GND				
36	CSI_DN3	MIPI CSI	Input	A18	
37	PCIE_RX_N	PCIe	Input	A19	
38	CSI_DP3	MIPI CSI	Input	B18	
39	PCIE_RX_P	PCIe	Input	B19	
40	GND				
41	GND				

J1					
Number	Signal	Power Logic	Input/Output	CPU Ball	Note
42	PCIE_TX_N	PCle	Output	A20	
43	PCIE_CLK_N	PCle	Input	A21	
44	PCIE_TX_P	PCle	Output	B20	
45	PCIE_CLK_P	PCle	Input	B21	
46	GND				
47	GND				
48	USB1_DN	USB	In/Out	A22	
49	UART4_TXD	3.3V	In/Out	F18	M4 Debug UART
50	USB1_DP	USB	In/Out	B22	
51	UART4_RXD	3.3V	In/Out	F19	M4 Debug UART
52	GND				
53	USB1_ID	1.8V	Input	D22	Connected to GND or Unconnected
54	USB2_DN	USB	In/Out	A23	
55	USB1_VBUS	USB	Power Detect	F22	Connect USB 5V
56	USB2_DP	USB	In/Out	B23	
57	USB2_VBUS	USB	Power Detect	F23	Connect USB 5V
58	BOOT_MODE0	3.3V	Input	G26	
59	GND				
60	BOOT_MODE1	3.3V	Input	G27	10K pull-up 3.3V

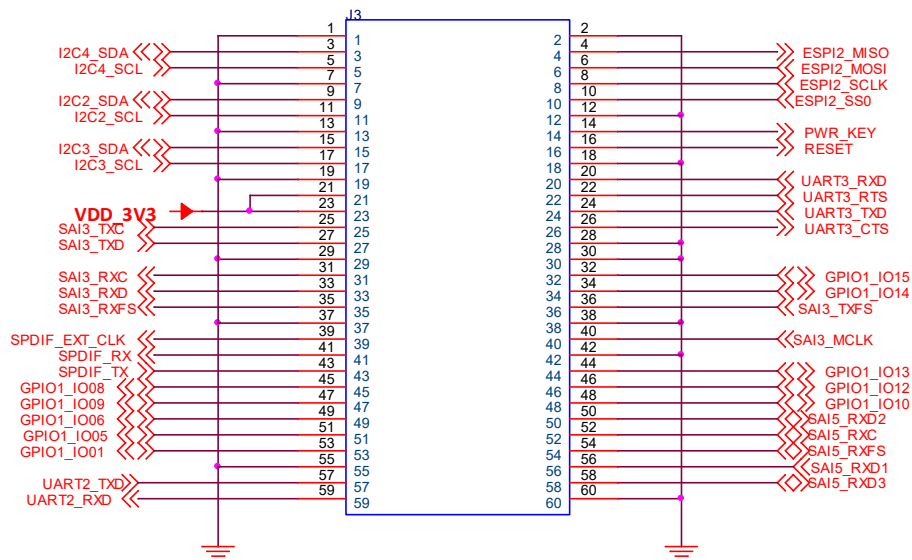


J2

Table2 Pin Definition Of J2

J2					
Number	Signal	Power Logic	Input/Output	CPU Ball	Note
1	GND				
2	SAI5_MCLK	3.3V	In/Out	AD15	
3	SAI1_RXD0	3.3V	In/Out	AG15	Boot CFG 0
4	GND				
5	SAI1_RXD1	3.3V	In/Out	AF15	Boot CFG 1
6	SAI5_RXD0	3.3V	In/Out	AD18	
7	SAI1_RXFS	3.3V	In/Out	AG16	
8	SAI1_TXC	3.3V	In/Out	AC18	
9	SAI1_RXC	3.3V	In/Out	AF16	
10	GND				
11	SAI1_RXD2	3.3V	In/Out	AG17	Boot CFG 2
12	SAI1_MCLK	3.3V	In/Out	AB18	
13	SAI1_RXD3	3.3V	In/Out	AF17	Boot CFG 3
14	GND				
15	SAI1_RXD4	3.3V	In/Out	AG18	Boot CFG 4
16	SAI1_TXFS	3.3V	In/Out	AB19	
17	SAI1_RXD5	3.3V	In/Out	AF18	Boot CFG 5
18	SAI2_MCLK	3.3V	In/Out	AD19	
19	SAI1_RXD6	3.3V	In/Out	AG19	Boot CFG 6
20	GND				
21	SAI1_RXD7	3.3V	In/Out	AF19	Boot CFG 7
22	SAI2_RXC	3.3V	In/Out	AB22	
23	SAI1_TXD0	3.3V	In/Out	AG20	Boot CFG 8
24	SD2_DATA0	NVCC_SD2	In/Out	AB23	
25	SAI1_TXD1	3.3V	In/Out	AF20	Boot CFG 9
26	SD2_DATA1	NVCC_SD2	In/Out	AB24	
27	SAI1_TXD2	3.3V	In/Out	AG21	Boot CFG 10
28	SD2_CMD	NVCC_SD2	In/Out	W24	
29	SAI1_TXD3	3.3V	In/Out	AF21	Boot CFG 11
30	GND				
31	SAI1_TXD4	3.3V	In/Out	AG22	Boot CFG 12
32	SAI1_TXD6	3.3V	In/Out	AG23	Boot CFG 14
33	SAI1_TXD5	3.3V	In/Out	AF22	Boot CFG 13
34	SAI1_TXD7	3.3V	In/Out	AF23	Boot CFG 15
35	SD2_RESET_B	NVCC_SD2	In/Out	AB26	
36	NVCC_SD2		Power output		
37	SD2_CD_B	NVCC_SD2	In/Out	AA26	
38	GND				
39	SD2_WP	NVCC_SD2	In/Out	AA27	
40	SD2_CLK	NVCC_SD2	In/Out	W23	

J2					
Number	Signal	Power Logic	Input/Output	CPU Ball	Note
41	GND				
42	GND				
43	LED_10_100	ETH_2V5	In/Out	24	AR8035
44	SD2_DATA3	NVCC_SD2	In/Out	V23	
45	LED_ACT	ETH_2V5	In/Out	21	AR8035
46	SD2_DATA2	NVCC_SD2	In/Out	V24	
47	LED_1000	ETH_2V5	In/Out	22	AR8035
48	GND				
49	ETH_TRP2	Analog	In/Out	15	AR8035
50	ETH_TRP0	Analog	In/Out	9	AR8035
51	ETH_TRN2	Analog	In/Out	16	AR8035
52	ETH_TRN0	Analog	In/Out	10	AR8035
53	GND				
54	GND				
55	ETH_TRP3	Analog	In/Out	18	AR8035
56	ETH_TRP1	Analog	In/Out	12	AR8035
57	ETH_TRN3	Analog	In/Out	19	AR8035
58	ETH_TRN1	Analog	In/Out	13	AR8035
59	ETH_2V5		Power output		Just for Ethernet LED
60	GND				



J3

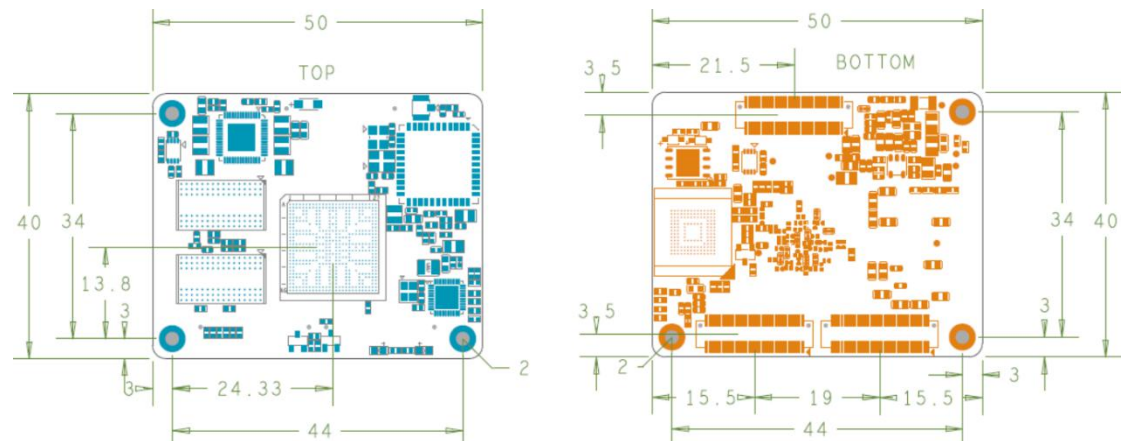
Table3 Pin Definition Of J3

J3					
Number	Signal	Power Logic	Input/Output	CPU Ball	Note
1	GND				
2	GND				
3	I2C4_SDA	3.3V	In/Out	E13	4.7K pull-up 3.3V
4	ESPI2_MISO	3.3V	In/Out	A8	
5	I2C4_SCL	3.3V	In/Out	D13	4.7K pull-up 3.3V
6	ESPI2_MOSI	3.3V	In/Out	B8	
7	GND				
8	ESPI2_SCLK	3.3V	In/Out	E6	
9	I2C2_SDA	3.3V	In/Out	D9	4.7K pull-up 3.3V
10	ESPI2_SS0	3.3V	In/Out	A6	
11	I2C2_SCL	3.3V	In/Out	D10	4.7K pull-up 3.3V
12	GND				
13	GND				
14	PWR_KEY		Input	A25	100K pull-up 1.8V
15	I2C3_SDA	3.3V	In/Out	F10	4.7K pull-up 3.3V
16	RESET		Input	40	BD71847MWV
17	I2C3_SCL	3.3V	In/Out	E10	4.7K pull-up 3.3V
18	GND				
19	GND				
20	UART3_RXD	3.3V	In/Out	D6	
21	VDD_3V3		Power output		
22	UART3_RTS	3.3V	In/Out	B6	
23	VDD_3V3		Power output		
24	UART3_TXD	3.3V	In/Out	B7	
25	SAI3_TXC	3.3V	In/Out	AG6	
26	UART3_CTS	3.3V	In/Out	A7	
27	SAI3_TXD	3.3V	In/Out	AF6	
28	GND				
29	GND				
30	GND				
31	SAI3_RXC	3.3V	In/Out	AG7	
32	GPIO1_IO15	3.3V	In/Out	AB9	
33	SAI3_RXD	3.3V	In/Out	AF7	
34	GPIO1_IO14	3.3V	In/Out	AC9	
35	SAI3_RXFS	3.3V	In/Out	AG8	
36	SAI3_TXFS	3.3V	In/Out	AC6	
37	GND				
38	GND				
39	SPDIF_EXT_CLK	3.3V	In/Out	AF8	

J3					
Number	Signal	Power Logic	Input/Output	CPU Ball	Note
40	SAI3_MCLK	3.3V	In/Out	AD6	
41	SPDIF_RX	3.3V	In/Out	AG9	
42	GND				
43	SPDIF_TX	3.3V	In/Out	AF9	
44	GPIO1_IO13	3.3V	In/Out	AD9	
45	GPIO1_IO08	3.3V	In/Out	AG10	
46	GPIO1_IO12	3.3V	In/Out	AB10	
47	GPIO1_IO09	3.3V	In/Out	AF10	
48	GPIO1_IO10	3.3V	In/Out	AD10	
49	GPIO1_IO06	3.3V	In/Out	AG11	
50	SAI5_RXD2	3.3V	In/Out	AD13	
51	GPIO1_IO05	3.3V	In/Out	AF12	
52	SAI5_RXC	3.3V	In/Out	AC15	
53	GPIO1_IO01	3.3V	In/Out	AF14	
54	SAI5_RXFS	3.3V	In/Out	AB15	
55	GND				
56	SAI5_RXD1	3.3V	In/Out	AC14	
57	UART2_TXD	3.3V	In/Out	E15	A53 Debug UART
58	SAI5_RXD3	3.3V	In/Out	AC13	
59	UART2_RXD	3.3V	In/Out	F15	A53 Debug UART
60	GND				

4. Mechanical Dimension

- Size: 50 x 40 x 7.3 mm
- PCB Parameter: 8 layer design, lead-free soldering process
- Weight: 12g



5. Electrical Characteristics

5.1 Working Temperature

Specification	Minimum Operating Temperature (°C)	Maximum Operating Temperature (°C)
Commercial Grade	0	70
Industrial Grade	−40	+85

6. Power Supply And System Resets

6.1 Power Source

The i.MX 8M Mini series processors have built-in power management function, So is only need to provide a +5V power source to the SOM-IMX8M-MINI via the 5V input pins of the J1 connector.

The power consumption is requested at least 2A/5V(10 W) for the IMX8M-MINI-SOM board to be working properly.

6.2 Power Control and Monitoring

Power control and monitoring on the IMX8M MINI SOM is implemented using the ROHM Power Control Integrated Circuit (PMIC) BD71847MWV-E2, designed specifically for the NXP i.MX8M MINI family of application processors.

The BD71847MWV-E2 provides Dynamic Voltage Scaling via I²C bus and/or digital input PMIC_STBY_REQ. The PMIC is accessible on the i.MX8M I2C1 bus for read and write at addresses 0x97 and 0x96, respectively.

6.3 System power

The SOM requires 5V as power input (at 5V_IN). The SOM then generates the local voltage rails for all SOM components through on-board PMICs.

- Power supply: 5V +/- 0.3V

Caution:

- (1) Do not connect the ETH_2V5/ VDD_3V3/ NVCC_SD2 power output pins to any high current devices or you might brownout the system. These power lines are shared with internal SOM circuits, so there is no safe limit for a high current device, but you can safely use them for low current tasks such as for a level shifter or pullup/down.
- (2) Do not connect any of the 3.3V I/O pins to a device that draws more than 82 mA of power or you will brownout the system.
- (3) You must provide a cooling solution to ensure the SOM surface maintains an operational temperature as specified in the environmental reliability section. You can use the SOM's threaded standoffs to mount a passive or active cooling solution.

6.4 Power Consumption Typical Values

The following table lists the power draw for certain SOM components during different operational tests.

It is only a reference value, the actual values also relates to the sources of the SOM module you are using.

Operational Test	SOM Power Values
Sleep	
Idel	
High Performance	

7. System Resets

7.1 Reset Architecture Overview

The SOM-IMX8M-MINI implements a reset architecture that ensures that the microprocessor is reset as appropriate on various hardware and software events.

The following is the types of reset.

7.2 Power-on Reset

This type of reset occurs when the power is initially applied to the SOM-IMX8M-MINI. As the supply voltage rises, the on-board PMIC holds the i.MX 8M MINI in reset until all the processor power supply voltages have risen above the appropriate voltage thresholds (90% of the nominal values). The internal power-on reset generation is disabled.

7.3 Brown-out Reset

In case any processor supply falls below/rises above its 80%/130% of its nominal voltage level, the PMIC generates a reset of the i.MX 8M MINI. After the brown-out reset has occurred, the PMIC holds the i.MX 8M in reset until all the supplies return to the range 90-110% of their nominal values.

7.4 Software Reset

This type of reset is activated by software running on the SOM through performing the i.MX 8M MINI software reset sequence.

7.5 External Reset

To activate this type of reset, a baseboard drives low the SYS_nRST signal on the IMX 8M MINI SOM interface connectors. Activating this signal leads to the i.MX8M MINI SOM power cycle.

8. Boot Mode

Use the BOOT_MODE[1:0] pins to configure the SOM boot mode setting as indicated in the following tables. The default configure is Internal boot.

Table4 Boot Mode

BOOT_MODE1	BOOT_MODE0	Boot type
0	0	Boot from fuses
0	1	Serial downloader
1	0	Internal boot, BOOT_CFG[15:0] are used to enable boot configure.
1	1	Reserved

The boot configuration is specified by the iMX8M MINI SOC, so for more details, refer to the iMX8M MINI SOC documentation.

9. Application

- HMI
- Medical appliances
- Industrial automation
- Weighing Scales
- Smart Toll Systems
- Educational Consoles

10. Trace impedance recommendations

The following table lists the recommended impedance for high-speed signals on the baseboard.

Table5 Trace Impedance Recommendation

Signal group	Impedance	PCB manufacture tolerance
All single-ended signal, unless specified	50 Ohm single-ended	+/-10%
PCIe TX/RX data pair	85 Ohm differential	+/-10%
PCIe differential clocks	100 Ohm differential	+/-10%
USB differential signals	90 Ohm differential	+/-10%
Ethernet Differential signals	100 Ohm differential	+/-10%
MIPI DSI	100 Ohm differential	+/-10%
MIPI CSI	100 Ohm differential	+/-10%

11. High-speed signal trace length compensation

The following table lists the trace length of high-speed signals, including MIPI CSI, MIPI DSI, PCIE, USB and Giga Ethernet. Those signals are high-speed signals that require the total etched trace lengths to be equal to each other. Due to space constraints on the SOM, the trace length of those signals currently are not equal. You must incorporate the length difference on your baseboard such that the trace length for all high-speed signals match each other.

Table6 Trace Length Compensation Of SOM

Name	Etch length(mils)	Manhattan length(mils)
MIPI CSI		
CSI_CKN	648.69	602.09
CSI_CKP	652.53	634.84
CSI_DN0	660.12	621.78
CSI_DP0	664.04	621.78
CSI_DN1	499.98	464.3
CSI_DP1	504.4	464.31
CSI_DN2	492.11	444.62
CSI_DP2	490.91	477.36
CSI_DN3	639.01	615.15
CSI_DP3	643.82	654.53
MIPI DSI		
DSI_CKN	515.05	503.66
DSI_CKP	519.04	503.67
DSI_DN0	510.88	523.35
DSI_DP0	515.6	523.35
DSI_DN1	653.06	661.15
DSI_DP1	657.2	661.15
DSI_DN2	665.93	641.46
DSI_DP2	668.04	641.47

DSI_DN3	511.74	483.98
DSI_DP3	516.23	483.98
PCIe		
PCIE_CLK_N	495.48	477.35
PCIE_CLK_P	495.7	516.73
PCIE_RX_N	475.14	457.67
PCIE_RX_P	487.48	497.04
PCIE_TX_N	623.25	634.84
PCIE_TX_P	649.18	674.21
USB1		
USB1_DN	647.78	654.52
USB1_DP	652.37	693.9
USB2		
USB2_DN	676.18	693.89
USB2_DP	680.79	733.26
Ethernet		
ETH_TRN0	246.14	172.62
ETH_TRP0	250.02	208.05
ETH_TRN1	225.73	145.06
ETH_TRP1	225.39	149
ETH_TRN2	373.36	408.84
ETH_TRP2	377.4	412.78
ETH_TRN3	348.17	397.03
ETH_TRP3	350.36	400.97

12. Circuit Example

12.1 Reset In

For the reset pin J3.16, a reset button to pull this pin to ground to reset core board is necessary, the ESD component and bypass capacitor is used according to the actual design, a resistor pull up to power supply is installed on SOM board, so not any resistors pull up/down is need.

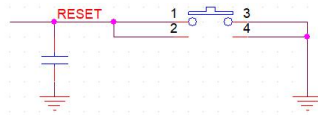


Figure1 Reset In

12.2 Power Key

For the power pin J3.14, assert this pin to ground to indicate a power event. Long press to turn off the SOM board and short press to turn on the SOM board. The ESD component and bypass capacitor is used according to the actual design, a resistor pull up to power supply is installed on SOM board, so not any resistors pull up/down is need.

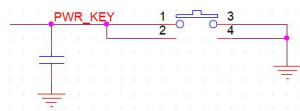


Figure2 Power Key

12.3 Boot Mode

The power used for pull up resistors for boot configuration should source from SOM board to avoid any unpredictable failure. The power output pins are J3.21 and J3.23.

The following figure shows to boot up from eMMC on SOM board.

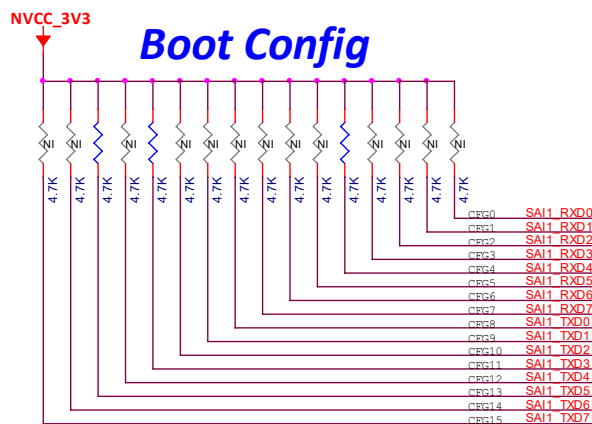


Figure3 Boot up from the eMMC on SOM

If the designer desires to boot the board up from any other storage device, please refer the following table to change the boot-up configuration, further information please refer to **i.MX 8M Mini Applications Processor Reference Manual**.

Caution: The pull-up resistor of boot configuration should be connected to VDD_3V3 from J3.

On-board eMMC: Connected to uSDHC3 8 bit

TF single on BTB connector: Connected to uSDHC2

On-board QSPI Flash: Connected to QSPI, 1.8V 64M bit QSPI flash, W25Q64FW

i.MX8M Mini ROM Fuse

Address		7	6	5	4	3	2	1	0
	0x470[15:8]	BOOT_CFG[15]	BOOT_CFG[14]	BOOT_CFG[13]	BOOT_CFG[12]	BOOT_CFG[11]	BOOT_CFG[10]	BOOT_CFG[9]	BOOT_CFG[8]
	0x470[15:8]	Infiniit-Loop (Debug USE only) 0 - Disable 1 - Enable	001 - SD/eSD			Port Select: 00 - uSDHC1 01 - uSDHC2 10 - uSDHC3		Power Cycle Enable: '0' - No power cycle '1' - Enabled via	SD Loopback Clock Source Sel (for SDR30 and SDR104 only) '0' - through SD pad '1' - direct
	0x470[15:8]		010 - MMC/eMMC						
	0x470[15:8]		011 - NAND			Pages in Block: 00 - 128 01 - 64 10 - 32 11 - 256		Nand_Row_address_bytes: 00 - 3 01 - 2 10 - 4 11 - 5	
	0x470[15:8]		100 - QSPI			Flash Auto Probe	FLASH_TYPE 000-Device supports 38 read by default 001-Device supports 48 read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MMC Octal DDR		
	0x470[15:8]		110 - SPI NOR			Port Select: 000 - eCSPI1 001 - eCSPI2 010 - eCSPI3			SPI Addressing: 0 - 3-bytes (24-bit) 1 - 2-bytes (16-bit)
	0x470[15:8]	Others - Reserved for future use							
		BOOT_CFG[7]	BOOT_CFG[6]	BOOT_CFG[5]	BOOT_CFG[4]	BOOT_CFG[3]	BOOT_CFG[2]	BOOT_CFG[1]	BOOT_CFG[0]
SD/eSD	0x470[7:0]	Fast Boot: 0 - Regular 1 - Fast Boot	Reserved	Reserved	Bus Width: 0 - 1-bit 1 - 4-bit	Speed 000 - Normal/SDR12 001 - High/SDR25 010 - SDR50 011 - SDR104 101 - Reserved for DDR50 Others - Reserved			Reserved
MMC/eMMC	0x470[7:0]		Bus Width: 000 - 1-bit 001 - 4-bit 010 - 8-bit 101 - 4-bit DDR (MMC 4.4) 110 - 8-bit DDR (MMC 4.4) Else - reserved.			Speed 00 - Normal 01 - High 10 - Reserved for HS200 11 - Reserved		USDHC IO VOLTAGE SELECTION For Normal Boot Mode 0 - 3.3V 1 - 1.8V	USDHC IO VOLTAGE SELECTION For Manufacture Mode 0 - 3.3V 1 - 1.8V
NAND	0x470[7:0]	BT_TOGGLEMODE	BOOT_SEARCH_COUNT: 00 - 2 01 - 2 10 - 4 11 - 8		Toggle Mode 33MHz Preamble Delay, Read Latency: '000' - 16 GPMICLK cycles. '001' - 1 GPMICLK cycles. '010' - 2 GPMICLK cycles. '011' - 3 GPMICLK cycles. '100' - 4 GPMICLK cycles. '101' - 5 GPMICLK cycles. '110' - 6 GPMICLK cycles. '111' - 7 GPMICLK cycles. '1111' - 15 GPMICLK cycles.				Reserved
FlexSPI	0x470[7:0]	HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms		FLASH Auto Probe Type		FlexSPI FLASH Dummy Cycle			
SPINOR	0x470[7:0]	CS select SPI only: 00 - CS#0 default 01 - CS#1 10 - CS#2 11 - CS#3	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved

Figure4 Table For Boot Configure

12.4 Giga Ethernet

Use a 0.1uF capacitor as bypass capacitor connect to TCT and RCT of the transformer but do not connect these pins to any power supply.

The 49.9R and capacitor matching networks are not necessary to the differential network. The designer should decide using these resistors and capacitors or not according to their design. For LED_ACT Pin that is J2.45, parallel LED output for 10/100/1000 BASE-T activity, active blinking. LED active low and is 3.3V tolerated.

For LED_1000 Pin that is J2.47, parallel LED output for 1000 BASE-T link, LED active low and is 3.3V tolerated.

For LED_10_100 Pin that is J2.43, parallel LED output for 10/100 BASE-T link. LED active low and is 3.3V tolerated.

Symbol	10M Link	10M Active	100M Link	100M Active	1000M Link	1000M Active
LED_10_100	OFF	OFF	ON	ON	OFF	OFF
LED_1000	OFF	OFF	OFF	OFF	ON	ON
LED_ACT	ON	BLINK	ON	BLINK	ON	BLINK

NOTE: Notes: on = active; off = inactive

Figure5 LED Status

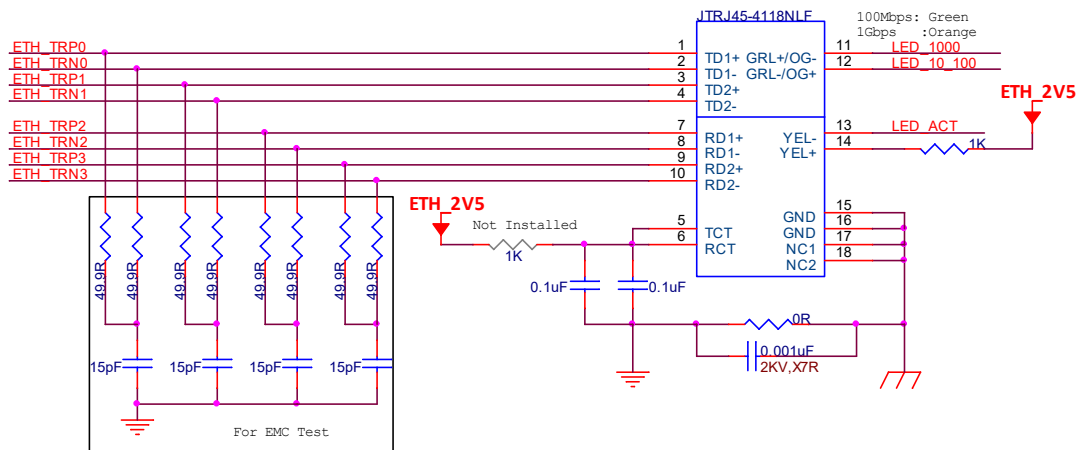


Figure6 GBE Demo

12.5 TF Card

It is strongly recommended that use the power source NVCC_SD2 output from J2.36 to power the high speed memory card, and NVCC_SD2 DO NOT use to power other devices. The voltage level of NVCC_SD2 can be changed through software to support the high speed mode. Note that maximum current output is 150mA. Do not exceed 150mA at any time to avoid any unpredictable failure.

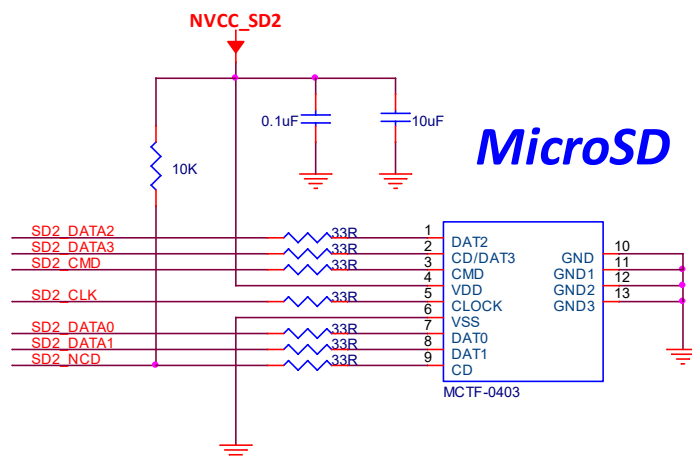
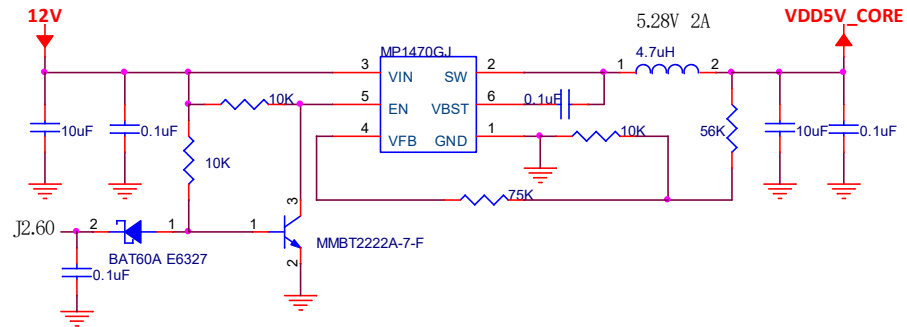


Figure7 TF Card Design Demo

12.6 SOM Power-Up Enable

Suggest that using J2.60 (GND) on SOM to enable the 5V power supply for SOM as the following demo circuit. There will be no 5V power supply from the BTB connector on Baseboard while no SOM installed, it can protect SOM board from hog plug-in.



GPIO1_IO05: During reset: output high without PU/PD; After reset: input with PU

SAI5_CLK: During reset: input without PU/PD; After reset: input with PD